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10/699,686	11/04/2003	Wolfgang Korber	Q78259	4926

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EXAMINER	
WONG, XAVIER S	
ART UNIT	PAPER NUMBER
2416	
MAIL DATE	DELIVERY MODE
12/22/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/699,686	KORBER ET AL.	
	Examiner	Art Unit	
	Xavier Szewai Wong	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27th August 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claim **1** have been considered but are *not persuasive.*

Applicants alleged that Merchant et al do not teach "a memory unit organized as a number of physical memory queues" where "each queue is assigned to an output port."

Merchant et al *clearly* mention "a first memory unit having a plurality of inputs, a plurality of outputs and a plurality of queues (col. 10 lines 14-15)," thus, such reads on as "a memory unit organized as a number of physical memory queues" since the first memory unit does comprise of queues; Merchant et al further *clearly* mention "inputs [are] being destined for predetermined ones of said first unit outputs (col. 10 lines 18-19)," thus, such reads on "each queue is assigned to an output port" since a *predetermined* output is, directly or indirectly, linked to a particular input through a queue. In addition, "input and output queues having *one-to-one* association" is well-known in the art of communication as evidently cited in col. 1 lines 31-33 of Merchant et al.

The limitations are read by Merchant et al at the *broadest* interpretation of the limitations presented as interpreted above and the applicants are further reminded that the claims are interpreted in light of the specification, limitations from the specification are *not* read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims **1**, **8**, **9**, **10**, **13** and **14** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Nong** (**US 2003/0123468 A1**) in view of **Merchant** et al (**US 5,408,463**).

Consider claim **1**, **Nong** discloses a multi-channel network node (fig. *2* @ *111*) for routing and switching data from a number of input ports (fig. 2 @ input ports) to a number of output ports (fig. *2* @ output ports). Data is buffered in an input port wherein the data is organized into physical buffers ([0057]: 14-18; fig. *5* @ buffers B11-B14); each of the buffer being assigned to a destined output port (fig. *4* @ buffers B11-B14); a switch fabric (fig. *2* @ *230*) that routes the data from the input port (comprising the data buffers) to the output port ([0057]: 8-12). Nonetheless, **Nong** may not have specifically disclosed a single memory unit organized as a number of physical queues. **Merchant** et al teach a single buffer memory unit comprising a plurality of N queues wherein the buffer memory unit stores incoming cells from a plurality of inputs 112-$_{1\sim N}$ and forwards cells to outputs 114-$_{1\sim N}$, wherein each individual input corresponds to a corresponding queue which, on a one-to-one basis, outputs to a corresponding output of the buffer memory unit (col. *2* ln. *53-60*, col. *10* ln. *14-40*). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the single buffer memory unit structure of **Merchant** et al to the switch memory of **Nong** to recognize synchronization among output queues.

Consider claim **8**, as applied to claim **1**, **Nong**, as modified by **Merchant** et al, shows in figure *3* a crossbar (matrix) switch *230* ([0052]).

Consider claim **9**, as applied to claim **1**, **Nong**, as modified by **Merchant** et al, discloses in figure *2* a scheduling controller *240* for controlling the switch *230* ([0051]: 4-14), which is a processor obviously controlled by software.

Consider claim **10**, as applied to claim **1**, **Nong**, as modified by **Merchant** et al, shows in figures *4*, *5* and *6* that input and output interfaces are assigned to the input and output ports respectively.

Consider claim **13**, as applied to claim **1**, **Nong** shows in figure *2* that node *111* output ports output data through speed-data paths (OSUDP) and subsequently in figure *1*, node *111* output data to an end user e.g. *132* or another node e.g. *112*. The output ports, thus, are output ports of the network node *111*.

Consider claim **14**, **Nong** discloses a multi-channel network node (fig. *2* @ *111*) for routing and switching data from any input port to any output port (figs. *4-6*) comprising steps of: queuing data into an input port wherein the data is organized into physical buffers ([0057]: 14-18; fig. *5* @ buffers B11-B14); each of the buffer being assigned to a destined output port (fig. *4* @ buffers B11-B14); a switch fabric (fig. *2* @ *230*) that routes the data from the input port (comprising the data buffers) to the output port ([0057]: 8-12). **Nong** may not have explicitly disclosed receiving data from a data channel by a *receiver unit*; or, the buffers (queues) constituting a "memory unit." **Merchant** et al teach in figure *1* a receive line interface, a single buffer memory unit comprising a plurality of N queues wherein the buffer memory unit stores incoming cells from a plurality of inputs $112_{1\sim N}$ and forwards cells to outputs $114_{1\sim N}$, wherein each individual input corresponds to a corresponding queue which, on a one-to-one basis, outputs to a corresponding output of the buffer memory unit (col. *2* ln. *53-60*, col. *10* ln. *14-40*). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the receiving unit and the single buffer memory unit

structure of **Merchant** et al to the switch memory of **Nong** to recognize synchronization among output queues.

Claim **5** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Nong** (**US 2003/0123468 A1**) in view of **Merchant** et al (**US 5,408,463**), as applied to claim **1**, and in further view of **Knorpp** et al (**US 4,947,387**).

Consider claim **5**, as applied to claim **1**, **Nong**, as modified by **Merchant** et al, disclose the claimed invention except do not specifically mention each memory queue is assigned to a memory agent controlling the operation of the memory queue. **Knorpp** et al show in figure *1* that each buffer store (queue) is controlled by an individual buffer store control (agent) (col. *2* ln. *4-14*). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement an agent control to each buffer queue as taught by **Knorpp** et al to the buffer memory unit queues of **Nong** and **Merchant** et al to ensure each buffer queue sends their data to their corresponding outputs regardless asynchronous and regardless of operations on other queues.

Claims **2** and **15** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Nong** (**US 2003/0123468 A1**) in view of **Merchant** et al (**US 5,408,463**), as applied to claims **1** and **14**, and in further view of **Bohm** et al (**US 2002/0027816 A1**).

Consider claims **2** and **15**, as applied to claims **1** and **14**, **Nong**, as modified by **Merchant** et al, discloses the claimed invention except explicitly mentioning the memory queues comprising a number of coherent memory cells. **Bohm** et al disclose utilizing coherent memory cells array (**[0055]**: 7-12). It would have been obvious to one of ordinary skill in the art when the invention was made to incorporate the coherent

memory cells of **Bohm** et al to the memory buffers of **Nong**, as modified by **Merchant** et al, for providing sufficient space for carrying out read/write operations in switches.

Claim **3** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Nong** (**US 2003/0123468 A1**) in view of **Merchant** et al (**US 5,408,463**) and **Bohm** et al (**US 2002/0027816 A1**), as applied to claim **2**, and in further view of **Strehler** (**US 5,122,984**).

Consider claim **3**, as applied to claim **2**, **Nong**, as modified by **Merchant** et al and **Bohm** et al, disclose the claimed invention except explicitly mentioning resizable memory cells. **Strehler** teaches the concept of sizable (re-sizable) memory cells (col. 1: 28-38). It would have been obvious to one of ordinary skill in the art when the invention was made to incorporate the teachings of **Strehler** to the invention of **Nong**, as modified by **Merchant** et al and **Bohm** et al, for organizing data structures to be stored (e.g. redistributing capacity among cells).

Claim **4** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Nong** (**US 2003/0123468 A1**) in view of **Merchant** et al (**US 5,408,463**), as applied to claim **1**, and in further view of **Kothary** (**US 6,249,528 B1**).

Consider claim **4**, as applied to claim **1**, **Nong**, as modified by **Merchant et al**, discloses the claimed invention except specifying a re-assembly unit coupled to the input ports of the node and the switch; and a segmentation unit with the memory unit and output ports of the node. **Kothary** shows in figure *2* a re-assembly unit coupled to a switch unit, which is coupled to a segmentation unit. The re-assembly unit in figure *13*

and the segmentation unit in figure *14* both show FIFO buffers (memory units) *152* and *166* respectively (col. 13: 52-67; col. 14: 42-57). It would have been obvious to one of ordinary skill in the art when the invention was made to incorporate the memory unit / re-assembly / segmentation units of **Kothary** to the invention of **Nong**, as modified by **Merchant** et al, for cell re-assembly and segmentation purposes.

Claim **6** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Nong** (**US 2003/0123468 A1**) in view of **Merchant** et al (**US 5,408,463**) and **Knorpp** et al (**US 4,947,387**), as applied to claim **5**, **Dooley** et al (**US 2002/0163922 A1**).

Consider claim **6**, as applied to claim **5**, **Nong**, as modified by **Merchant** et al and **Knorpp** et al, discloses the claimed invention except may not have *explicitly* shown the memory queue and agents form the switching unit. **Dooley** et al disclose an input switch port (fig. *1* @ *14*) comprise a traffic manager (fig. *2A* @ *22* → *agent*) and inside of the traffic manager comprises memory queues (fig. 3 @ 37) which leads to the switch interface (fig. *2* @ *24*) and eventually to the switch (fig. *1* @ *16*) ([0026]). It would have been obvious to one of ordinary skill in the art when the invention was made to incorporate the input switch port of **Dooley** et al to the node of **Nong**, as modified by **Merchant** et al and **Knorpp** et al, so the queues coordinate with the traffic manager to switch the queues to the corresponding output ports.

Claim **7** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Nong** (**US 2003/0123468 A1**) in view of **Merchant** et al (**US 5,408,463**) and **Knorpp** et al (**US**

4,947,387), as applied to claim **5**, and in further view of **Fujii** et al (**US 2003/0014264 A1**).

Consider claim **7**, as applied to claim **5**, **Nong**, as modified by **Merchant** et al and **Knorpp** et al, discloses the claimed invention except specifically mentioning the memory queues and agent operate *asynchronously* and *in parallel*. **Fujii** et al disclose an input/output processing unit (control / agent) asynchronously inputs data stream into a FIFO memory queue in a decode processing unit wherein both input/output and decode processing units operate in parallel to each other ([0212]). It would have been obvious to one of ordinary skill in the art to apply the concept of a control unit operating asynchronously and in parallel with a queue as taught by **Fujii** et al to the buffers and manager (agent) of **Nong**, as modified by **Merchant** et al and **Knorpp** et al, for efficient parallel processing of data.

Claims **11** and **12** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Nong** (**US 2003/0123468 A1**) in view of **Merchant** et al (**US 5,408,463**), as applied to claim **1**, and in further view of **Liebowitz** et al (**US 5,757,784**).

Consider claim **11**, as applied to claim **1**, **Nong**, as modified by **Merchant** et al, discloses the claimed invention except explicitly mentioning a burst buffer being utilized in the node. **Liebowitz** et al disclose in figure *4* the usage of burst buffer *68* in a fragment assembler/disassembler FAD *66* (col. 4: 19-41). It would have been obvious to one of ordinary skill in the art when the invention was made to combine the burst buffer

of **Liebowitz** et al to the node of **Nong**, as modified by **Merchant** et al, for efficiently handling different data sizes and formats.

Consider claim **12**, as applied to claim **11**, **Nong**, as modified by **Merchant** et al and **Liebowitz** et al, shows in figures *2* that the output port *220* (fig. *9* output port → memory unit) is coupled with switch *230*.

Claim **16** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Nong** (**US 2003/0123468 A1**) in view of **Merchant** et al (**US 5,408,463**), as applied to claim **1**, and in further view of **Moriwaki** et al (**EP 0,918,419 A2**).

Consider claim **16**, and as applied to claim **1**, **Nong**, as modified by **Merchant** et al, discloses the claimed invention except specifically disclosing a network of interactive *cascaded* multi-channel nodes. **Moriwaki** et al teach the concept of different levels of inputs and outputs in the ATM switch system from the input highways of the cell distributors to the ATM switches to the output highways of the cell assemblers; therefore, creating a cascade of devices operating in a succession of stages (col. *3* lines *52-58* & col. *4* lines *1-46*; fig. *1*). The ATM switch units exchange (interaction) cells with other ATM switch units in an N x N switch matrix (col. *6* lines *6-39*; *abstract*; fig. *1*). It would have been obvious to one of ordinary skill in the art when the invention was made to apply the concept of **Moriwaki** et al to the invention of **Nong**, as modified by **Merchant** et al, for inter-node communications.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Dell et al, US 2002/0085578 A1: Three-stage switch fabric with buffered crossbar devices wherein a one-to-one relationship between the routing queues in the input stage and the routing queues in the output stage [0007]

Colmant et al, US 2002/0196778 A1: a switch resorts to a crossbar-like mode of operation when the almost-full threshold is exceeded, because then only one input is allowed to send to an active output, such as there is a one-to-one matching between (active) inputs and outputs, just like in a crossbar. Note also that both shared memory grant as well as per-destination grant are determined on a per-input basis [0063]

THIS ACTION IS MADE **FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Xavier Wong whose telephone number is 571-270-1780. The examiner can normally be reached on Monday through Friday 8 am - 5 pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Xavier Szewai Wong/
x.s.w
15th December 2008

/Kevin C. Harper/
Primary Examiner, Art Unit 2416